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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,910	03/12/2004	Hong-Jyh Li	2004P50029US/I331.135.101	8291

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EXAMINER	
HOANG, QUOC DINH	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,910	LI ET AL.	
	Examiner	Art Unit	
	Quoc D. Hoang	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/12/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of claims 1-17 in the reply filed on 10/03/2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-7, 9-12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paton et al., (US Pat No. 6,703,277 hereinafter "Paton") in view of Kim et al., (US Pat No. 6,621,114 hereinafter "Kim").

Regarding claim 1, Paton teaches a semiconductor device comprising;

a substrate 102 including active regions (col. 9, lines 15-20 and Fig. 4B);

a high-k material layer 108 implanted with a species, the high-k material layer 108 proximate the substrate 102 (col. 9, lines 30-45 and Fig. 4B); and

a gate electrode 110 proximate the high-k material layer 108 (col. 11, lines 22-29 and Fig. 4B).

Paton teaches the substrate 102 including active regions, but does not teach the substrate including isolation regions.

However, Kim teaches a substrate 102 including isolation regions 121 (col. 5, lines 40-55 and Fig. 3). Since Paton and Kim are all from the same field of endeavor, the purpose disclosed by Kim would have been recognized in the pertinent art of Paton. It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to provide isolation regions in order to electrically isolate transistor from other integrated circuit devices within the semiconductor substrate as taught by Kim, column 1, lines 50-55.

Regarding claim 2, Paton teaches wherein a transistor is formed from the substrate 102, the high-k material layer 108, and the gate electrode 110 (col. 11, line 27 and Fig. 4B).

Regarding claim 3, Paton teaches further comprising:

a pre-gate material layer 118 between the substrate 102 and the high-k material layer 108 (col. 9, lines 35-40 and Fig. 4B).

Regarding claim 4, Paton teaches wherein the pre-gate material layer 118 comprises SiO_2 (col. 9, lines 35-40 and Fig. 4B).

Regarding claim 5, Paton teaches wherein the pre-gate material layer 118 has a thickness up to about 10 Angstroms (col. 10, line 57).

Regarding claim 6, Paton teaches further comprising:

a buffer layer 120 between the high-k material layer 108 and the gate electrode 110 (col. 10, lines 60-65 and Fig. 4B).

Regarding claim 7, Paton teaches wherein the buffer layer 120 comprises TiSi (col. 11, lines 13-16, titanium silicate).

Regarding claim 9, Paton teaches wherein the species comprises nitrogen (col. 10, line 30).

Regarding claim 10, Paton teaches wherein the high-k material layer 108 comprises one of HfO_2 (col. 10, line 2).

Regarding claim 11, Paton teaches wherein the high-k material layer 108 has a thickness within the range of 20 to 200 Angstroms (col. 9, line 63).

Regarding claim 12, Paton teaches wherein the high-k material layer 108 has a thickness within the range of 20 to 200 Angstroms (col. 9, line 63), but does not teach the thickness within the range of 3 to 20 Angstroms. Although Paton's thickness is not the claimed range, this does not define patenable over Paton since the etching ratio is well known processing variable and the discovery of the optimum or workable range involves only routine skill in the art.

Regarding claim 14, Kim teaches wherein the isolation regions 121 comprise trench isolation regions (col. 1, line 55). Since Paton and Kim are all from the same field of endeavor, the purpose disclosed by Kim would have been recognized in the pertinent art of Paton. It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to provide isolation regions in order to electrically isolate transistor from other integrated circuit devices within the semiconductor substrate as taught by Kim, column 1, lines 50-55.

4. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Paton et al., (US Pat No. 6,703,277 hereinafter "Paton") and Kim et al., (US Pat No. 6,621,114 hereinafter "Kim") as applied to claim 6 above, and further in view of Yu (US Pat No. 6,867,101).

Paton teaches a buffer layer 120 between the high-k material layer 108 and the gate electrode 110 (col. 10, lines 60-65), but does not teach wherein the buffer layer has a thickness within the range of 10 to 200 Angstroms.

However, Yu teaches a buffer layer 22 between the high-k material layer 30 and the gate electrode 32 and the buffer layer 22 has a thickness within the range of 1-2 atomic layer (col. 3, lines 45-67 and Fig. 6). Since Paton and Yu are all from the same field of endeavor, the purpose disclosed by Yu would have been recognized in the pertinent art of Paton. It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to provide thin nitride buffer layer 22 in order to provide sufficient diffusion resistance as well as thermal stability in a thin feature size as taught by Yu, column 2, lines 15-21. Although Yu's thickness of the buffer layer is not the claimed range, this does not define patenable over Yu since the etching ratio is well known processing variable and the discovery of the optimum or workable range involves only routine skill in the art.

5. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Paton et al., (US Pat No. 6,703,277 hereinafter "Paton") and Kim et al., (US Pat No. 6,621,114

hereinafter "Kim") as applied to claim 1 above, and further in view of Kizilyalli et al (US Pat No. 6,320,238 hereinafter "Kizilyalli").

Paton teaches the high-k material layer 108 implanted with a species (nitrogen), (col. 9, lines 30-45 and Fig. 4B), but does not teach wherein a dose of the implanted species is within the range of $1x10^{13}$ ions/cm^2 to $1x10^{16}$ ions/cm^2.

However, Kizilyalli teaches a high-k material layer 108 implanted with a nitrogen at a suitable dose (col. 5, lines 1-15 and Fig. 1). Since Paton and Kizilyalli are all from the same field of endeavor, the purpose disclosed by Kizilyalli would have been recognized in the pertinent art of Paton. It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to provide high-k material layer implanted with a nitrogen at a suitable dose in order to reduce the gate dielectric thickness to facilitate device scaling and integration as taught by Kizilyalli, column 2, lines 15-20. Although Kizilyalli's dose of the implanted species is not the claimed range, this does not define patenable over Kizilyalli since the concentration is well known processing variable and the discovery of the optimum or workable range involves only routine skill in the art.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 15-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Paton et al., (US Pat No. 6,703,277 hereinafter "Paton").

Regarding claim 15, Paton teaches a transistor comprising;

a gate electrode 110 (col. 11, lines 22-29 and Fig. 4B);

a high-k gate dielectric layer 108 implanted with a species, the high-k gate dielectric layer 108 proximate the gate electrode 110 (col. 9, lines 30-45 and Fig. 4B); and

a substrate 102 comprising an active region, the substrate 102 proximate the high-k gate dielectric layer 108 (col. 9, lines 15-20 and Fig. 4B) .

Regarding claim 16, Paton teaches further comprising:

a buffer layer 120 between the high-k material layer 108 and the gate electrode 110 (col. 10, lines 60-65 and Fig. 4B).

Regarding claim 17, Paton teaches wherein the gate electrode 110 comprises polysilicon (col. 11, line 23).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quoc Hoang whose telephone number is (571) 272-1780. The examiner can normally be reached on Monday-Friday from 8.00 AM to 5.00 PM.

If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone numbers of the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quoc Hoang
Patent examiner/AU 2818

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